嵌入式系統導論

1.

Consider a 1Kx8 RAM chip (i.e., it has 1024bytes).

(1) How many address lines and data lines are there in the chip?

(2) How many such chips do you need to construct a 16Kx16 memory?

(3) What Kind of decoder do you need to connect this 16Kx16 memory?

2.

Explain “Big endian” and “Little endian” with an example?

Hint：Consider the following C program:

```
#include<stdio.h>
int main() {
        unsigned char buf[]={1,2,3,4};
        short *p = (short*)buf;
        printf("==%hd\n", *p);    return 0;
}
```

Discuss the output of this program if you run it on a Big-Endian machine? and what if run it on a Little Endian machine?

3.

Assume the integer a contains 38 and integer b contains 49.

What would be the result of a and b after doing the following 3 statements:

```
a = a xor b;
b = a xor b;
a = a xor b;
```

4.

Assume that *$s1* and *$s2* are used for the input and both initially contain the integers a and b, respectively. Assume that *$v0* is used for the output.

```
        add     $t0, $zero, $zero
loop:   beq     $s2, $zero, finish
        add     $t0, $t0, $s1
        sub     $s2, $s2, 1
        j       loop
finish: addi    $t0, $t0, 100
        add     $v0, $t0, $zero
```

Please describe in one mathematic formula what it computes (in terms of a, b).

5. 簡單說明:

a.) 何謂阻抗匹配 (impendence match)？

b.) What is Open-Drain ?

Pin Name	28L PDIP/ SOIC	24L QFN	Pin Type	Standard Function
GPB0	3	24	I/O	Bidirectional I/O Pin (5.5 volt tolerant inputs: open-drain outputs). Can be enabled for interrupt on change, and/or internal pull-up resistor.
GPB1	4	2	I/O	Bidirectional I/O Pin (5.5 volt tolerant inputs: open-drain outputs). Can be enabled for interrupt on change, and/or internal pull-up resistor.

c.) What is Setup time and hold time?

			600	—		1.8V ≦ Vcc ≦ 5.5V
11	TSU:WP	WP setup time	4000 600	— —	ns	1.7V ≦ Vcc < 1.8V 1.8V ≦ Vcc ≦ 5.5V
12	THD:WP	WP hold time	4700 600	— —	ns	1.7V ≦ Vcc < 1.8V 1.8V ≦ Vcc ≦ 5.5V
13	TAA	Output valid from clock **(Note2)**	—	3500	ns	1.7V ≦ Vcc < 1.8V

6. 簡單比較:

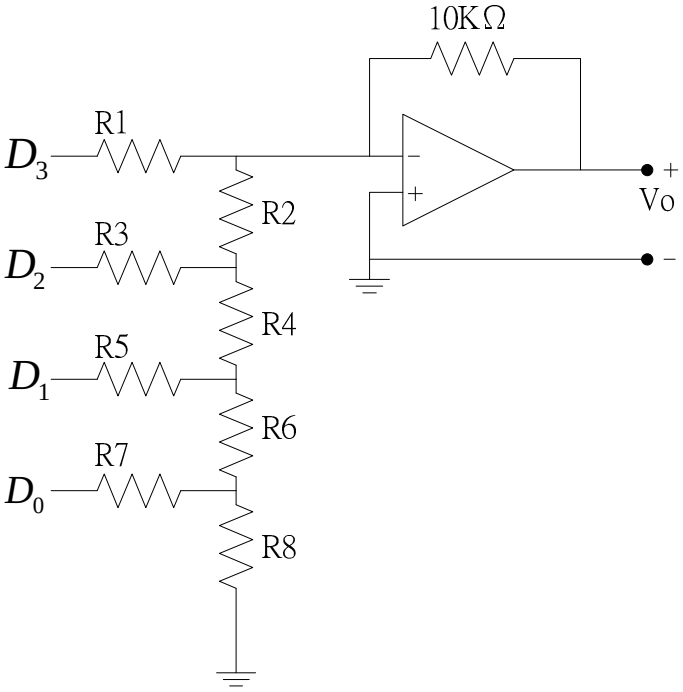
(1) IC family: TTL vs. CMOS

(2) CPU family: RISC vs CISC

7. [Electronics]

An OP AMP is used in the circuit of 4-bit digital/analogue converter (DAC) shown below. D_3~D_0 are digital signals with logic '1' of 5V and logic '0' of 0V. Please find the resistance R1~R8 to make the output analogue voltage V_0 to be:

$$V_0 = -\left(\frac{1}{3}\right)[D_3 \times 2^3 + D_2 \times 2^2 + D_1 \times 2^1 + D_0 \times 2^0]\ V$$



8. [Operating system].

Consider a virtual memory system with the following properties:

- 12-bit virtual byte address
- 256-byte pages
- 65536 bytes of physical memory

The system uses a single level page table. The contents of the page table are ***partially*** shown below (where VPN: Virtual page number and PPN: Physical page number).

VPN	Valid	PPN	VPN	Valid	PPN
0	0	-	6	1	6
1	1	0xfd	7	0	7
2	1	0x48	8	0	-
3	0	-	9	1	0xfe
4	1	0x55	A	1	0xf2
5	1	0x32	B	0	

(i)What is the total size of the page table for each process on this machine, assuming that the valid, protection, dirty, and use bits take a total of 4 bit and that all the virtual pages are in use?

(ii) Please convert the following virtual addresses into physical addresses:
0xae2, 0x258.